# VLSI Lab 1 – DAC

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## Schematic

### Resistor Divider Schematic

A computer screen shot of a black background

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### 5 Bit Dac Schematic

A screenshot of a computer

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### DAC Output Resistance

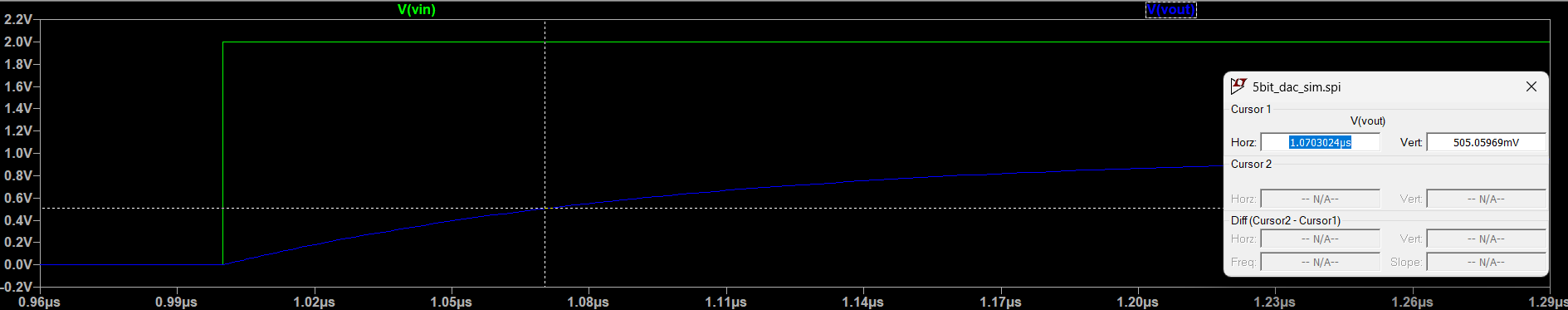
The output resistance of a voltage divider is the resistance of each resistor in parallel (). Stacking voltage dividers in the way done in this DAC puts the next divider in the chain in series with the lower resistor connected to ”bot” and in parallel with the input resistor connected to “in”. Assuming is the resistor connected to b1, is connected to “bot”, and is the calculated output resistance of the next voltage divider, the resistance of a 2 bit DAC would be . This can be chained up to N bits, but the resistance of the last extra 10k resistor on the lsb should be added.

It turns out that because , always evaluates to and , causing the total output resistance to always be equal to , or 10k in this case.

### Delay, driving a load

Predicted output delay:

Matches spice sim:



### Simulations

If the DAC drives a 10k load its output voltage will get halved since its output resistance is 10k.

## Layout

### 10k Resistor

You select the width of a resistor based on your manufacturers minimum feature width, then calculate your length based on the formula .

A blue and yellow lines on a white background

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### DRC & NCC

A white text with black text

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